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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,117	09/28/2000	Hideo Miyake	1614.1082	8617

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EXAMINER
KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/671,117	MIYAKE ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 20* is/are allowed.

6)☒ Claim(s) *1-13, 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1-13, 15, 17-20 are presented for examination. Claims 18-20 have been added and claims 14 and 16 have been canceled. This office action is in response to the amendment filed on 10/15/02.

Claim Objections

2. Claims 7 and 19 are objected to because of the following informalities:

As to claim 7 has been amended in the version with marking (Page 10), however the claim has not been properly amended in the amendment section.

As to claim 19, line 6, "clocks" should be changed to -- blocks-- for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald US Patent No. 5,913,224 and in view of Ekner et al. (Ekner) US Patent No.

6092159.

As to claim 1, MacDonald discloses a method of controlling a cache memory (Fig. 2 Ref. 200) connected to a main memory (Fig. 2 Ref. 300) and divided into a plurality of cache blocks (Fig. 2 Ref. 220) comprising: supplying a lock signal (Fig. 2 Ref. 230 and col. 7 line 5 thru col. 8 line 20) and performing either reading or writing (col. 7 lines 27-29) of the main memory when the replace inhibition state is set by the lock signal, replacing the at least one of the cache blocks to the main memory is inhibited during the reading aor writing of the main memory (col. 7 lines 28-30) but does not discloses a lock signal generated on the basis of a lock instruction.

However, Ekner discloses a lock signal generated on the basis of a lock instruction (abstract) for the purpose of easy of modification over a hard wired operation.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify a lock signal of MacDonald to a lock signal generated on the basis of a lock instruction as disclosed by Ekner because it would allow to easy of modification over the hard wired logic.

As to claim 2, MacDonald further discloses at least on of flags corresponding to the cache blocks (Fig. 2 Ref. 230).

As to claim 3, MacDonald further discloses unlock instruction (Fig. 2 Ref. 230 and col. 7 lines 56-58). Ekner further discloses unlock instruction (abstract).

As to claim 18, MacDonald further discloses unlock instruction (Fig. 2 Ref. 230 and col. 7 lines 56-58). Ekner further discloses unlock instruction (abstract).

As to claim 4, MacDonald discloses a computer including a main memory and a cache memory (Fig. 2), the cache memory being connected to the main memory and divided into a plurality of cache blocks (Fig. 2) comprising: a block setting unit which supplies a lock (Fig. 2 Ref. 230 and col. 7 line 5 thru col. 8 line 20) and reading/ writing unit (col. 7 lines 27-29), when the replace inhibition state is set by the lock signal, replacing the at least one of the cache blocks to the main memory is inhibited during the reading aor writing of the main memory (col. 7 lines 28-30) but does not discloses a lock signal generated on the basis of a lock instruction.

However, Ekner discloses a lock signal generated on the basis of a lock instruction (abstract) for the purpose of easy of modification over a hard wired operation.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify a lock signal of MacDonald to a lock signal generated on the basis of a lock instruction as disclosed by Ekner because it would allow to easy of modification over the hard wired logic.

As to claim 5, MacDonald further discloses at least on of flags corresponding to the cache blocks (Fig. 2 Ref. 230).

As to claim 6 , Ekner further discloses unlock instruction (abstract). MacDonald further discloses unlock instruction (Fig. 2 Ref. 202 and col. 7 lines 56-58).

As to claim 7, MacDonald discloses a method of controlling a cache memory (Fig. 2 Ref. 200) connected to a main memory (Fig. 2 Ref. 300) and divided into a plurality of cache blocks (Fig. 2 Ref. 220), which is executed by a computer (Fig. 2 Ref. 100) that accesses the main memory through the cache memory (Fig. 2), comprising: determining that an address designated by the instruction matches with an address of att least one of the cache blocks of the cache memory (read hit and read miss reads on this limitation, col. 7 lines 24-44) and supplying a lock/unlock signal (Fig. 2 Ref. 230 and col. 7 line 5 thru col. 8 line 20), replacing at least one of the cache blocks to the main memory of the peripheral system is inhibited (col. 7 lines 56-57) but does not discloses a lock/unlock instruction.

However, Ekner discloses a lock/unlock instruction (abstract) for the purpose of easy of modification over a hard wired operation.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify a lock/unlock signal of MacDonald to a lock/unlock instruction as disclosed by Ekner because it would allow to easy of modification over the hard wired logic..

As to claim 8, MacDonald discloses a computer including a main memory and a cache

memory (Fig. 2), the cache memory being connected to the main memory and divided into a plurality of cache blocks (Fig. 2) comprising: a comparator which determines that an address designated by an instruction matches with an address of at least one of the cache block (read hit and read miss reads on this limitation, col. 7 lines 24-44) and a lock/unlock control unit (Fig. 2 Ref. 230 and col. 7 line 5 thru col. 8 line 20) and reading/ writing unit (col. 7 lines 27-29), but does not discloses a lock/unlock instruction.

However, Ekner discloses a lock/unlock instruction (abstract) for the purpose of easy of modification over a hard wired operation.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify a lock/unlock signal of MacDonald to a lock/unlock instruction as disclosed by Ekner because it would allow to easy of modification over the hard wired logic.

As to claim 9, MacDonald further discloses a load control unit (Fig. 2 Ref. 202).

As to claim 10, MacDonald further discloses a store control unit (Fig. 2 Ref. 202).

As to claim 11 , MacDonald further discloses a flash control unit (Fig. 2 Ref. 202 and col. 7 lines 56-58).

As to claim 12 , MacDonald further discloses an invalidate control unit (Fig. 2 Ref. 202

and col. 7 lines 56-58).

As to claim 19, MacDonald discloses a method of controlling a cache memory (Fig. 2 Ref. 200) connected to a main memory (Fig. 2 Ref. 300) and divided into a plurality of cache blocks (Fig. 2 Ref. 220) comprising: supplying a lock and an unlock signals (Fig. 2 Ref. 230 and col. 7 line 5 thru col. 8 line 20) and performing either reading or writing (col. 7 lines 27-29) of the main memory when the replace inhibition state is set by the lock signal, replacing the at least one of the cache blocks to the main memory is inhibited during the reading aor writing of the main memory (col. 7 lines 28-30) but does not discloses a lock and an unlock instructions.

However, Ekner discloses a lock instruction and an unlock instruction (abstract) for the purpose of easy of modification over a hard wired operation.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify a lock and an unlock signals of MacDonald to a lock and an unlock instructions as disclosed by Ekner because it would allow to easy of modification over the hard wired logic.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 13 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Biggs et al. (Biggs) US Patent 5,410,669.

As to claim 13, Biggs discloses the invention as claimed. Biggs discloses a method of controlling a cache memory is connected to a main memory with a first address space and capable of acting as a random access memory, which is executed by a computer that accesses that main memory through that cache memory (Fig. 3 and col. 4 line 46 thru col 5 line 25) comprising the steps of: determining wether that cache memory is acting as the random access memory (col. 4 lines 54+) and assigning a second address space which separate from the first address space of the main memory for the cache memory when the cache memory is acting as the random access memory (col. 4 line 46 thru col 5 line 25) and a bus control unit (Fig. 1 Ref. 20) .

As to claim 17, Biggs discloses the invention as claimed above. Biggs a computer including a main memory and a cache memory (Fig. 1 Ref. 14), the main memory having a first address space (Fig. 1 Ref. 30) and the cache memory being capable of acting as a RAM (abstract) comprising: a determination unit (col. 4 line 46 thru col 5 line 25), an assignment unit (col. 4 line 46 thru col 5 line 25), a bus control unit (Fig. 1 Ref. 20), a peripheral system (Fig. 1 Ref. 22), and access control unit (abstract).

Allowable Subject Matter

7. Claims 15 and 20 are allowed.

Response to Amendment

8. Applicant's arguments filed on 10/15/02 have been fully considered but they are not deemed to be persuasive.

Applicant's remarks that the references not teaching a lock/unlock instruction is not considered persuasive. Ekner discloses a lock signal generated on the basis of a lock instruction (abstract). Therefore broadly written claims are disclosed by the references cited.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

12. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

14. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-Final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HONG CHONG KIM
PRIMARY EXAMINER

HK
Primary Patent Examiner
December 27, 2002